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July 28, 2000
Agent's Docket No. **UPA-00156**

Assistant Commissioner for Patents
Washington, D.C. 20231

Re: **U.S. Utility Patent Application**
Inventor: **Randy H. Y. Lo, Chi-Chuan Wu and Ssu-Cheng Lai**
Title: **Method Of Packaging Multi Chip Module**

Sir:

The above-identified utility patent application is transmitted herewith for filing:

Enclosed are:

1. **Fourteen(14)** sheets of specification, claims, and abstract.
2. **Six (6)** sheets of drawings containing FIGs. **1** through **3**.
3. An executed Declaration and Power of Attorney for Utility Patent Application.
4. An Information Disclosure.
5. A Credit Card Payment Form (PTO-2038) for the payment of **$1,050.00** to cover:
   (a) **Basic Utility Patent Filing Fee** $690;
   (b) **Claims in excess of twenty**: $18 x (40-20) = $360 (**three** independent claims and **thirty-seven** dependent claims).
6. A Recordation Form Cover Sheet and an Assignment which the Commissioner is requested to record and return to the undersigned.

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as Express Mail in an envelope addressed to: Box New Application, Assistant Commissioner for Patents, Washington, D.C. 20231, on the date shown below.

Date: July 28, 2000 Mail Label: EK446903745US

By: _____
Jason Z. Lin

7. A Credit Card Payment Form (PTO-2038) for the payment of **$40.00** to cover the **Assignment Recordation Fee**.

Please kindly acknowledge receipt of the above items by having your mailroom stamp and return the enclosed postcard.

Respectfully submitted,

Jason Z. Lin
Agent for Applicant
Reg. No. 37,492

METHOD OF PACKAGING MULTI CHIP MODULE

FIELD OF THE INVENTION

The present invention relates to a method of integrated circuit (IC) package, and particularly, to multi chip module package (MCM package) of low cost and high reliability to package a plurality of bare chip and CSP(Chip Scale Package) on a substrate so as to increase the package density.

BACKGROUND OF THE INVENTION

In conventional semiconductor manufacture, a wafer which is well treated is cut into a plurality of chips, and fixed on a frame by using gold (Au) wires to connect micro electrodes on the chip and pins of the lead frame. The above structure is then enclosed by suitable plastic to protect the internal semiconductor devices. The process to connect the chip to the lead frame and enclose is referred as packaging.

The present advanced package, such as CSP (chip scale package), becomes much smaller, lighter, thinner, and shorter compared with the conventional package, such as QFP (Quad Flat Pack) or SOP (Small Outline Package) in order to reduce the cost. Meanwhile, ceramic packaging has been gradually replaced by plastic packaging. The reliability of the product is further enhanced by multi layer interconnect structure, protection layer process, and high quality of packaging. To further reduce

the cost of package is greatly desired in the present IC industry. Therefore, advanced packaging such as CSP or wafer level CSP has been developed to increase the package density. MCM package is one of most promising techniques.

KGD is defined as the chip that meets the specification and passes the test without wiring. To increase the qualified ratio of MCM package in the semiconductor process, it is desired to use KGD in packaging. However, the use of KGD will increase the cost of packaging.

SUMMARY OF THE INVENTION

To overcome the above shortcoming in the conventional IC packaging, an object of the present invention is to provide a method of MCM package, which with CSPs as small and thin package bodies and integrates those bare chip and CSP into ball grid array package (BGA package) to greatly reduce the cost because CSP test has advantages of easy test and low cost compared with conventional KGD test.

Another object of the present invention is to provide a MCM package structure of low cost and high reliability, which includes a substrate, one or more chip package, a plurality of electrical connect pins, and a package material to enclose the substrate, the chip, and the chip package.

Other features and advantages of the invention will become apparent from the following description of the invention that refers to the accompanying drawings.

FIG. 1A is a schematic diagram of MCM package structure with wire bonding in the prior arts;

FIG. 1B is a schematic diagram of MCM package structure with flip chip bonding in the prior arts;

FIG. 2A is a schematic diagram of CSP package structure with wire bonding in the prior arts;

FIG. 2B is a schematic diagram of CSP package structure with flip chip bonding in the prior arts;

FIG. 2C is a schematic diagram of another CSP package structure with a central pad bonding in the prior arts;

FIG. 2D is a schematic diagram of wafer level CSP package in the prior arts;

FIG. 3A is a schematic diagram of the first embodiment of MCM package structure in the present invention, illustrating a CSP package with wire bonding and a CSP package with flip chip bonding;

FIG. 3B is a schematic diagram of the second embodiment of MCM package structure in the present invention, illustrating a CSP package with flip chip bonding and a CSP package with a central pad bonding;

FIG. 3C is a schematic diagram of the third embodiment of MCM package structure in the present invention, illustrating a bare chip with wire bonding and a CSP package with flip chip bonding;

FIG. 3D is a perspective view of the third embodiment of MCM

package structure in the present invention;

FIG. 3E is a schematic diagram of the fourth embodiment of MCM package structure in the present invention, illustrating a CSP package with wire bonding and a bare chip with flip chip bonding; and

FIG. 3F is a schematic diagram of the fifth embodiment of MCM package structure in the present invention, illustrating a CSP package with a central pad bonding and a bare chip with wire bonding.

DETAILED DESCRIPTION OF THE PREFEERED EMBODIMENT

FIGs. 1A and 1B show the structure of MCM package in the prior arts. The package body encloses a plurality of chips, which are interconnected by wire bonding or flip chip bonding. FIG. 1A schematically illustrates the package structure with wire bonding, which comprises a substrate 11, a plurality of chips 12, solder balls 13 under the substrate 11, wires 15 to connect the upper chip 121 and the substrate 11, and package mold resin 14. FIG. 1B schematically illustrates the package structure with flip chip bonding, which comprises a substrate 11, a plurality of chips 12, solder balls 13 under the substrate 11, ball bumps 16 to connect the lower chip 122 and the substrate 11, and package mold resin 14. Since the chips enclosed within the package are not examined by burn-in test and function test (F/T), the yield of the chips are not determined before packaging, and the yield of the package body after packaging can not promoted. If four chips are enclosed within the package body and each chip has an average

F/T yield 99%, the yield of the package is : (99%)X(99%)X(99%)X(99%) = 96%.

Therefore, the F/T yield of the whole MCM package reduces to 96% after packaging the four chips. The more the chips packaged in the package, the less the yield. It is disadvantageous for MCM package to apply to advanced IC packaging in the future.

In the prior arts, one solution to overcome the above disadvantage is to provide KGD. To prevent the F/T yield of the package from reducing due to undetermined yield of the chip, both burn-in test and function test are needed for the chips, which will be packaged in subsequent packaging process. Those chips pass through the above tests are call 'known-good dies', abbreviated as "KGDs". However, the KGD process is high cost because the size of the chip is very small and not easily fixed during burn-in test and function test.

The present invention provides an improved chip packaging method. FIGs. 2A-2D show CSP package structure in the prior arts. CSP is referred to the package that has a size just a little bigger than the chip and has a height less than 1.00 mm. FIG. 2A is a schematic diagram of CSP package structure with wire bonding in the prior arts, FIG. 2B is a schematic diagram of CSP package structure with flip chip bonding in the prior arts, FIG. 2C is a schematic diagram of another CSP package structure with a central pad bonding in the prior arts, and FIG. 2D is a schematic diagram of wafer level CSP in the prior arts. The CSP is not only light, thin, short,

and small, but also passes through burn-in test and function test so that the yield of the CSP is not an issue. It is important that the cost of burn-in test and function test of CSP process is much lower than that of the KGD process. Another aspect is that CSP has no yield issue and can easily replace KGD process to integrate into MCM package because of light, thin, short, and small size.

Therefore, thin and small CSP or wafer level CSP after testing is served as KGD, which may include bare chips. Those bare chips can connect to the substrate by wire bonding or flip chip bonding, and the chips and CSP are further integrated into ball grid array package (BGA package) so as to achieve the requirement of low cost and high quality for the MCM process.

[The first embodiment]

FIG. 3A illustrates the first embodiment of MCM package structure in the present invention,. in which the CSP package with wire bonding and flip chip bonding. The CSP is integrated into MCM package process, and includes a substrate 31, solder balls 33 under the substrate 31, package mold resin 34, the CSP body 371 with wire bonding and is electrically connected to the substrate 31, while the CSP 372 with flip chip bonding is electrically connected to the substrate 31.

[The second embodiment]

FIG. 3B illustrates the second embodiment of MCM package structure

in the present invention, in which the CSP package with flip chip bonding and central pad bonding. The MCM package includes a substrate 31, solder balls 33 under the substrate 31, package mold resin 34, the CSP 372 is electrically connected to the substrate 31, while the CSP 373 is electrically connected to the substrate 31 by the wire 35.

[The third embodiment]

FIG. 3C illustrates the third embodiment of MCM package structure in the present invention, in which CSP package with flip chip bonding. The MCM package includes a substrate 31, solder balls 33 under the substrate 31, package mold resin 34, the CSP body 372 is electrically connected to the substrate 31, while the bare chip 321 is electrically connected to the substrate 31 by the wire 35.

[The fourth embodiment]

FIG. 3E illustrates the fourth embodiment of MCM package structure in the present invention, in which the CSP package with wire bonding. The MCM package includes a substrate 31, solder balls 33 under the substrate 31, package mold resin 34, the. CSP body 371 is electrically connected to the substrate 31, while the bare chip 322 is electrically connected to the substrate 31.

[The fifth embodiment]

FIG. 3F illustrates the fifth embodiment of MCM package structure in the present invention, in which the CSP 373 package with a central pad bonding. The MCM package includes a substrate 31, solder balls 33 under the substrate 31, package mold resin 34, the. CSP 373 with a central pad bonding is electrically connected to the substrate 31 by the wires 35, while the bare chip 321 is electrically connected to the substrate 31 by the wires 35.

Although only the preferred embodiments of this invention were shown and described in the above description, it is requested that any modification or combination that comes within the spirit of this invention be protected.

WHAT IS CLAIMED IS:

1. A multi chip module package structure with low cost and high reliability, comprising:

a substrate;

a plurality of chip package bodies;

a plurality of electrical connect points, electrically connecting the chip package bodies and the substrate;

a plurality of electrical connect pins; and

a package material, enclosing the substrate, connect points, and chip package body.

2. The structure as claimed in claim 1, wherein said chip package body is a chip-scale package (CSP) or wafer level CSP.

3. The structure as claimed in claim 1, wherein at least one of said chip package bodies is a CSP with a wire bonding.

4. The structure as claimed in claim 1, wherein at least one of said chip package bodies is a CSP with a flip chip bonding.

5. The structure as claimed in claim 1, wherein at least one of said chip package bodies is a CSP with a central pad bonding.

6. The structure as claimed in claim 1, wherein said chip package bodies pass burn-in test and function test.

7. The structure as claimed in claim 2, wherein at least one of said chip package bodies is a CSP with a wire bonding.

8. The structure as claimed in claim 2, wherein at least one of said chip

package bodies is a CSP with a flip chip bonding.

9. The structure as claimed in claim 2, wherein at least one of said chip package bodies is a CSP with a central pad bonding.

10. The structure as claimed in claim 2, wherein said chip package bodies pass burn-in test and function test.

11. The structure as claimed in claim 1, wherein said plurality of electrical connect pins are solder balls.

12. The structure as claimed in claim 1, wherein said plurality of electrical connect points are solder balls or gold wires.

13. A multi chip module package structure with low cost and high reliability, comprising:

a substrate;

at least one chip;

one or more than one chip package bodies;

a plurality of electrical connect points, electrically connecting the chip package bodies and the substrate;

a plurality of electrical connect pins; and

a package material, enclosing the substrate, connect points, chips, and chip package bodies.

14. The structure as claimed in claim 13, wherein said chip is a bare chip.

15. The structure as claimed in claim 14, wherein at least one chip is bonded to the substrate by wire bonding or flip chip bonding.

16. The structure as claimed in claim 13, wherein said chip package body

is a chip-scale package (CSP) or wafer level CSP.

17. The structure as claimed in claim 13, wherein at least one of said chip package bodies is a CSP with a wire bonding.

18. The structure as claimed in claim 13, wherein at least one of said chip package bodies is a CSP with a flip chip bonding.

19. The structure as claimed in claim 13, wherein at least one of said chip package bodies is a CSP with a central pad bonding.

20. The structure as claimed in claim 13, wherein said chip package bodies pass burn-in test and function test.

21. The structure as claimed in claim 16, wherein at least one of said chip package bodies is a CSP with a wire bonding.

22. The structure as claimed in claim 16, wherein at least one of said chip package bodies is a CSP with a flip chip bonding.

23. The structure as claimed in claim 16, wherein at least one of said chip package bodies is a CSP with a central pad bonding.

24. The structure as claimed in claim 16, wherein said chip package bodies pass burn-in test and function test.

25. The structure as claimed in claim 13, wherein said plurality of electrical connect pins are solder balls.

26. The structure as claimed in claim 13, wherein said plurality of electrical connect points are solder balls or gold wires.

27. A method of packaging multi chip module at low cost and with high reliability to form multi chip module package containing a plurality of

chips bonded to a substrate as a main body, wherein said method is characterized as: using one or more than one chip package body as CSP, which is electrically connected to the substrate to form said main body.

28. The method as claimed in claim 27, wherein said main body may form a plurality of electrical connect pins and is enclosed by a package material.

29. The method as claimed in claim 28, wherein said plurality of electrical connect pins are solder balls.

30. The method as claimed in claim 27, wherein said chip package body is of chip-scale package (CSP) or wafer level CSP.

31. The method as claimed in claim 27, wherein at least one of said chip package bodies is a CSP with a wire bonding.

32. The method as claimed in claim 27, wherein at least one of said chip package bodies is a CSP with a flip chip bonding.

33. The method as claimed in claim 27, wherein at least one of said chip package bodies is a CSP with a central pad bonding.

34. The method as claimed in claim 27, wherein said chip package bodies pass burn-in test and function test.

35. The method as claimed in claim 30, wherein at least one of said chip package bodies is a CSP with a wire bonding.

36. The method as claimed in claim 30, wherein at least one of said chip package bodies is a CSP with a flip chip bonding.

37. The method as claimed in claim 30, wherein at least one of said chip package bodies is a CSP with a central pad bonding.

38. The method as claimed in claim 30, wherein said chip package bodies pass burn-in test and function test.

39. The method as claimed in claim 27, wherein said chip package body has a height less than 1.00 mm.

40. The method as claimed in claim 27, wherein said chip package body has a plurality of electrical connect points, which are solder balls or gold wires.

ABSTRACT

A method of packaging a multi chip module (MCM) with low cost and high reliability is disclosed. In the MCM process, a plurality of bare chips and CPSs, such as CPU or memory device, are integrated on a substrate to increase the package density. The method discards the high cost KGD process and directly takes the thin and small CSPs passing the tests as KGD and integrates the chips and CSPs into ball grid array package (BGA package) so that the cost is reduced and the yield and quality of the package is improved.

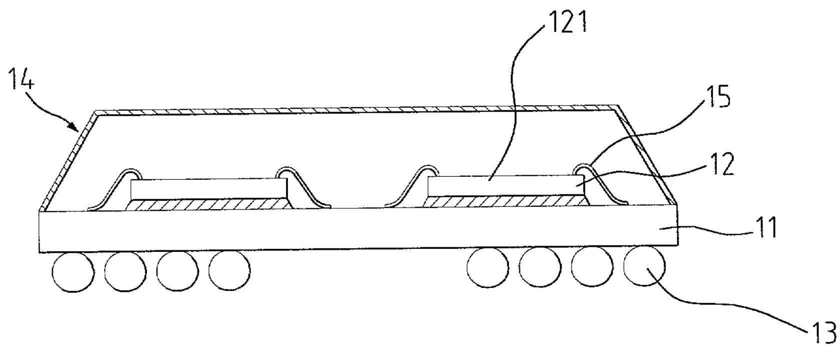

FIG.1A(Prior Art)

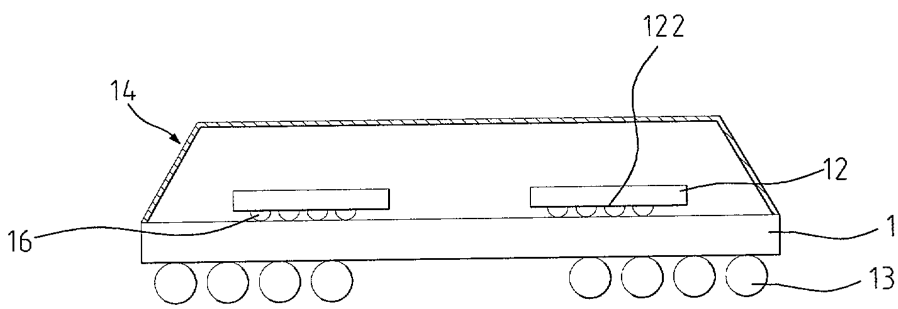

FIG.1B(Prior Art)

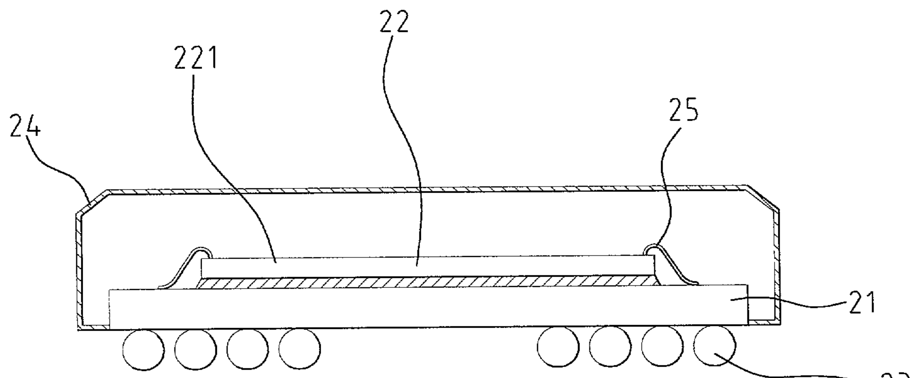

FIG.2A(Prior Art)

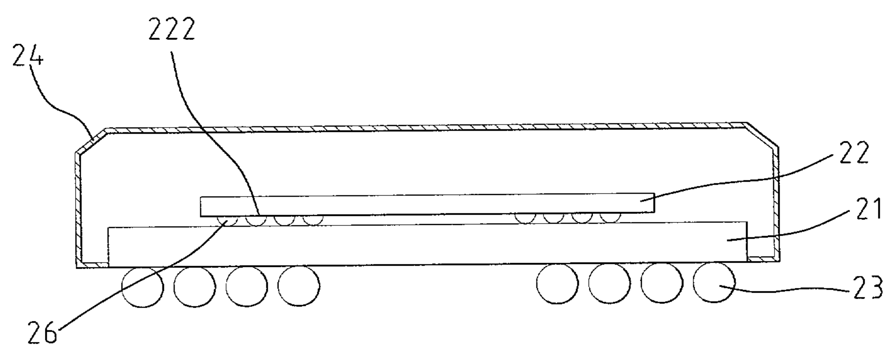

FIG.2B(Prior Art)

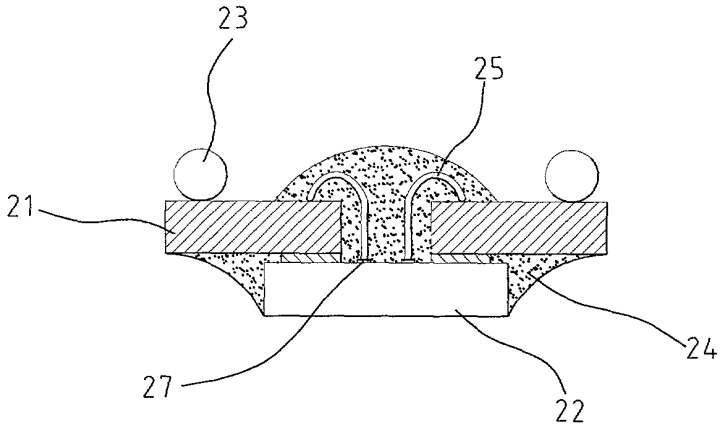

FIG.2C(Prior Art)

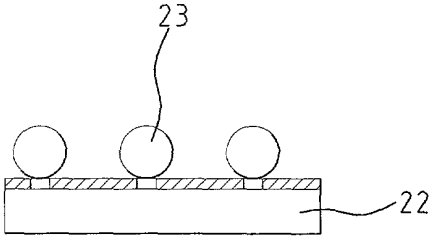

FIG.2D(Prior Art)

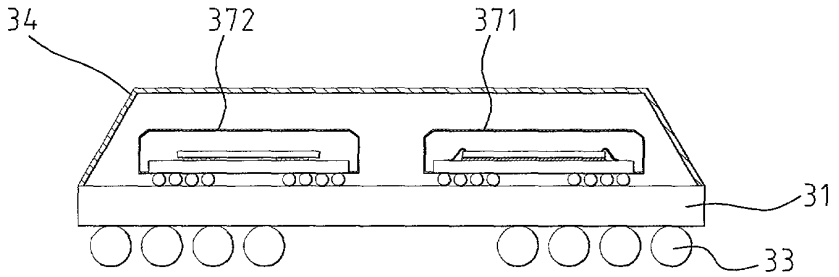

FIG.3A

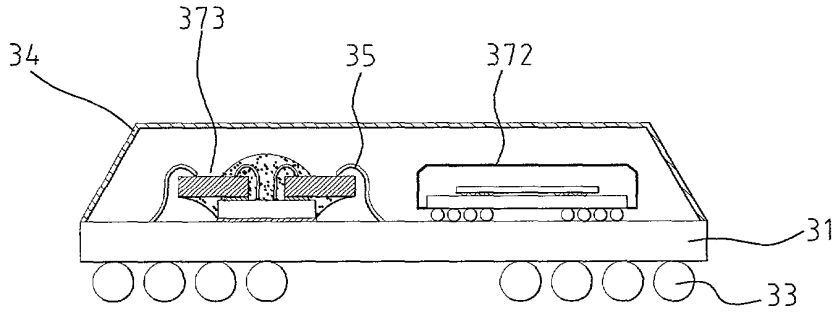

FIG.3B

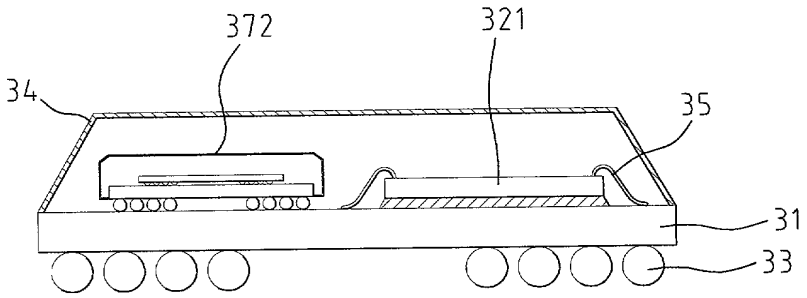

FIG.3C

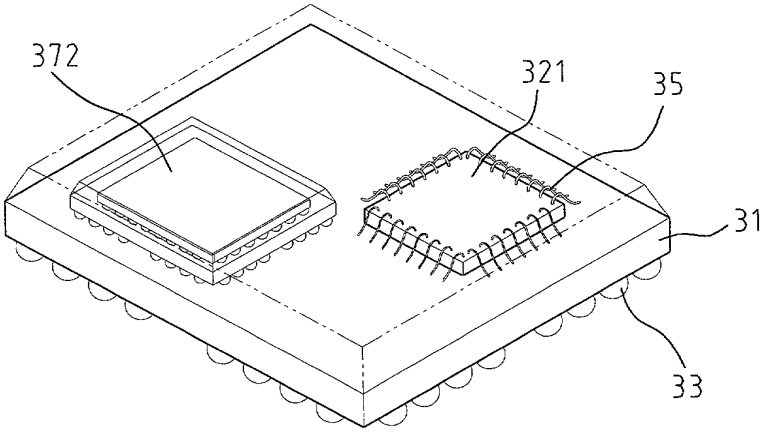

FIG.3D

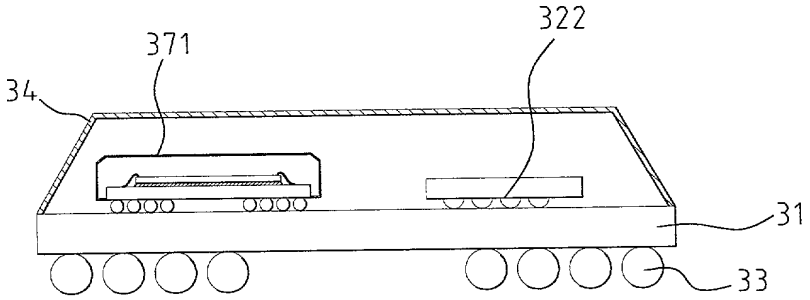

FIG.3E

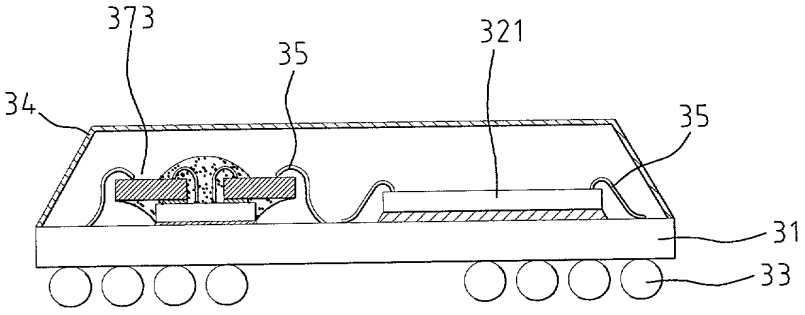

FIG.3F

UNITED STATES OF AMERICA COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION	FILE NO. UPA-00156

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name and that I verily believe that I am the original, first and sole inventor(if only one name is listed below) or an original, first and joint inventor(if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD OF PACKAGING MULTI CHIP MODULE

the specification of which is attached hereto, unless the following box is checked:

☐ was filed on _____ as United States patent application Serial Number _____, or PCT International patent application

No. _____ and was amended on _____ (if any).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to be material to patentability in accordance with Title 37, Code of Federal Regulations, Section 1 56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate or United States provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s) or Provisional Application(s)

COUNTRY	APPLICATION NUMBER	DATE OF FILING *(day, month, year)*	PRIORITY CLAIMED UNDER 35 U.S.C.119
			YES NO
			YES NO

I hereby claim the benefit under *Title 35, United States Code, Section 120* of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by *the first paragraph of Title 35, United States Code, Section 112.* I acknowledge the duty to disclose information which is material to patentability as defined in *Title 37, Code of Federal Regulations, Section 1.56* which became available between the filing date of the prior application and the national or PCT international filing date of this application.

UNITED STATES APPLICATION NUMBER	DATE OF FILING *(day, month, year)*	STATUS (patented, pending, abandoned)

I hereby appoint the agent(s), whose name(s) and Registration No(s). and address is list below/per attached, as my principal agent(s) with full power of substitution and revocation to prosecute this application, to transact all business in the Patent and Trademark Office connected therewith and to receive all correspondence.

SEND CORRESPONDENCE TO :

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Saratoga, CA 95070 **Fax: (408)867-7437**

I hereby declare that all statements made herein of my own knowledge are true and that all statement made on information and belief are believed to be true, and further that these statement were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under *Section 1001 of Title18 of the United States Code*, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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